Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. E**
2. **DO**
3. **QCC**
4. **Q0**
5. **Q1**
6. **Q2**
7. **Q3**
8. **Q4**
9. **Q5**
10. **NC**
11. **D**
12. **GND**
13. **CP**
14. **N. S**
15. **NC**
16. **Q6**
17. **Q7**
18. **Q8**
19. **Q9**
20. **Q10**
21. **Q11**
22. **NC**
23. **N. Q11**
24. **VCC**

**.068”**

**3**

**4**

**5**

**6**

**7**

**8**

**9**

**11**

**2 1 24 23**

**12 13**

**21**

**20**

**19**

**18**

**17**

**16**

**14**

**MASK**

**REF**

**.068”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: FLOAT**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .068” X .068” DATE: 9/23/21**

**MFG: ZYTREX THICKNESS .000” P/N: DM2504**

**DG 10.1.2**

#### Rev B, 7/1